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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,507	05/02/2005	Mihai Adrian Tiberiu Sanduleanu	NL 021080	4322

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EXAMINER	
PEREZ, JAMES M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
01/11/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/533,507	SANDULEANU ET AL.	
	Examiner	Art Unit	
	James M. Perez	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/2/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6853696) in view of Savoj (Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems), further in view of Yoon (Digital Logic Implementation of the Quadricorrelators for Frequency Detector).

With regards to claim 1, Moser teaches a Phase locked loop (PLL) (col. 1, lines 25-30, and 40-45) comprising a frequency detector including a quadricorrelator (fig. 2: col. 7, lines 7-16), the loop being characterized in that the quadricorrelator comprises clocked bi-stable circuits (fig. 2: elements 26a,b: col. 7, lines 30-35) coupled to multiplexers (fig. 2: element 28) being controlled by a signal having the same bit-rate as the incoming signal (fig. 2: elements 28, 32, and DATA: col. 6, lines 12-17).

Moser does not explicitly teach two limitations: Limitation 1) the use of double edge clocked bi-stable circuits and Limitation 2) the use of a balanced quadricorrelator.

Limitation 1)

Savoj teaches a frequency detector which uses double edge clocked bi-stable circuits (fig. 11: section 3.2.2: two double-edge-triggered flipflops).

Therefore it would be obvious to one of ordinary skill in the art at time of the invention to combine quadricorrelator frequency detection circuit of Moser with double-edge flipflop and frequency detection circuit of Savoj in order to provide an improved performance in frequency detector in order to better utilize a wider range of frequencies while reducing the required size of the circuitry.

Limitation 2)

Yoon teaches the use of a digital Balanced Quadricorrelator (fig. 6: Section V).

Therefore it would be obvious to combine the quadricorrelator frequency detection circuit of Moser with balanced quadricorrelator of Yoon in order to create an improved frequency detection circuit with double frequency detector gain (Section V: paragraphs 3-4).

With regards to claim 2, Moser in view of Savoj further in view of Yoon teach the limitation of claim 1.

Moser further teaches a first pair of clocked bi-stable (fig. 2: elements 26a,b: col. 7, lines 30-35) coupled to a first multiplexer (fig. 2: element 28) and a second pair of clocked bi-stable (fig. 2: elements 30a,b: col. 7, lines 36-49) coupled to a second multiplexer (fig. 2: element 32) are supplied by mutually quadrature phase shifted signals respectively to provide a first signal and a second signal indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals (fig. 2: col. 6, lines 12-49 and col. 7, lines 8-49).

Moser does not explicitly teach the use of double edge clocked bi-stable circuits.

Savoj teaches a frequency detector which uses double edge clocked bi-stable circuits (fig. 11: section 3.2.2: two double-edge-triggered flipflops).

Therefore it would be obvious to one of ordinary skill in the art at time of the invention to combine quadricorrelator frequency detection circuit of Moser with double-edge flipflop and frequency detection circuit of Savoj in order to provide an improved performance in frequency detector in order to better utilize a wider range of frequencies while reducing the required size of the circuitry.

With regards to claim 3, Moser in view of Wu teaches the limitation of claim 2.

Moser further teaches the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator (fig. 4: elements VCO, ICK and QCK).

Allowable Subject Matter

4. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Perez whose telephone number is 571-270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JP
1/7/2008

SHUWANG LIU
SUPERVISORY PATENT EXAMINER